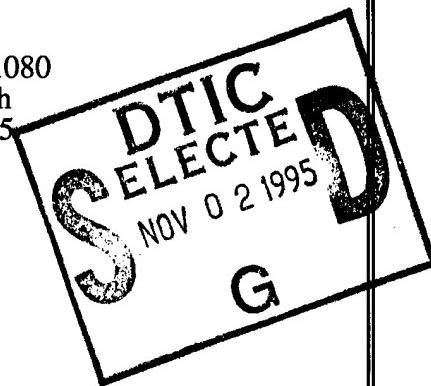


Quarterly Technical Report

**Defects and Impurities in 4H- and 6H-SiC
Homoepitaxial Layers: Identification, Origin,
Effect on Properties of Ohmic Contacts and
Insulating Layers and Reduction**

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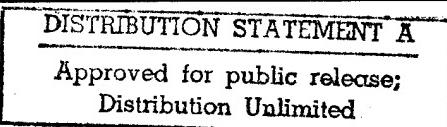
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The design and construction of a new and unique CVD system for the deposition and analysis of SiC thin films is underway. Initial measurements of the impact ionization coefficients of electrons and holes in SiC devices have been made. Degradation in breakdown voltage and an increase in the leakage current were observed. Analytical expressions were derived for the extraction of impact ionization coefficients from I-V data. Simulations were performed for a simple p-n junction diode, with and without impact ionization, and impact ionization coefficients were extracted using the analytical expressions derived. NiAl contacts with Ni passivating layers were deposited at room temperature on p-type 6H-SiC (0001) substrates. As-deposited contacts were rectifying with very low leakage current densities ($\sim 1 \times 10^{-8} \text{ A/cm}^2$ at 10 V), ideality factors between 1.4 and 2.4, and a Schottky barrier height (SBH) of approximately 1.37 eV. The contacts on $p^+ (1 \times 10^{19} \text{ cm}^{-3})$ were ohmic after annealing for 10-80 s at 1000 °C in a N ₂ ambient. The estimated specific contact resistivity from a non-mesa etched TLM pattern was $2-3 \times 10^{-2} \Omega \text{ cm}^2$. The Ni/NiAl contacts deposited on SiC with lower carrier concentrations ($1-5 \times 10^{18} \text{ cm}^{-3}$) were not ohmic after annealing at 1000 °C for 10-60 s but became nearly ohmic after annealing for 80 s. As-deposited Ni and Au contacts on p-type 6H-SiC displayed similar current-voltage characteristics with calculated SBH's of 1.31 and 1.27 eV, respectively. These ideality factors and SBH's are higher than for Ni contacts (and other previously studied contacts) on n-type 6H-SiC (0001). The higher ideality factors indicate that thermionic emission was not the dominant current transport mechanism in the p-type SiC and may indicate the occurrence of recombination at deep levels. Initial designs for a UHV compatible, combined cleaning via hydrogen plasma, SiH ₄ dosing and <i>in situ</i> vapor phase HF cleaning, oxidation and oxide deposition system for 6H-SiC(0001) wafers have been completed. The oxide formation will involve multi-step processing including plasma oxidation, plasma CVD, UHV thermal oxidation, and UHV CVD. A mask set has been designed to fabricate metal oxide-semiconductor gated diodes as a test of the interface electrical properties between insulators and SiC.			
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I. Introduction

The two most important materials-related problems affecting the performance of all SiC devices and their associated components (e.g., contacts) are the defects and the undesired impurities which become incorporated in the homoepitaxial SiC layers in which all devices are currently fabricated. Bhatnagar [1] has shown that the reverse blocking leakage current in high voltage Schottky diodes is three orders of magnitude higher than theoretically predicted as a result of defects in the epi-layer. The formation of micropipes, stepped screw dislocations, interacting dislocation loops, polyganized networks of dislocations and growth twins as well as stacking faults during the sublimation growth of SiC boules are likely the root cause of some of the defects in the epitaxial layer. However, with the exception of the micropipes, the types and concentrations of line, planar and other three-dimensional defects and their effect on the performance of devices and individual device components in the important epi-layer have not been similarly determined. As such, it is not known which of the latter defects actually are translated from the wafer into the epi-layer during its deposition and, therefore, should be vigorously controlled during boule growth and which defects are generated during deposition.

The relatively uncontrolled occurrence of the n-type donor of N and deep level compensating impurities such as Ti in the epilayer have been identified via secondary ion mass spectrometry, photoluminescence and cathodoluminescence investigations. However, the origins of essentially all of these impurities are unknown. For high-temperature, -power and -frequency devices, it is highly desirable to control or eliminate these impurities such as to attain undoped films with uncompensated carrier concentrations of 10^{14} cm^{-3} —two orders of magnitude lower than what is, at present, normally achieved in standard commercial depositions.

The formation of low resistivity and thermally stable ohmic contacts to 4H- and 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have an advantage over Si, the contact resistivities must be below $1 \times 10^{-5} \Omega\text{-cm}^2$, as noted by Alok, *et al.* [2]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on low melting point Al or Al alloys to dope the SiC surface below the contacts. These materials are not suitable for devices intended for high-temperature operation. While the fabrication of ohmic contacts to SiC has also normally depended on the attainment of a very heavily-doped near-surface region, the introduction during deposition of high levels of dopants in the near surface device region of the epi-layer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice.

Based on all of these issues and recent experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

To fabricate most microelectronic devices, the growth or deposition of stable insulators is needed to provide both passivating layers and gate dielectrics. Silicon carbide is almost invariably thermally oxidized, albeit at a slower rate, in the same manner and temperature range that is employed for Si. Most of the previous studies regarding the oxidation of SiC have been concerned with polycrystalline materials. It has been shown by Harris and Call [3] and Suzuki, *et al.* [4] that the (0001) face of 6H-SiC oxidizes according to the same linear-parabolic equation reported for Si by Deal and Grove [5]. The model states that the initial stage of oxidation is reaction rate limited and linear, but becomes parabolic as the diffusion of the oxidant through the oxide becomes the rate limiting factor. Research at NCSU by Palmour *et al.* [6] has demonstrated that the oxidation process on SiC in wet and dry oxygen and wet argon obeys the linear-parabolic law. Both wet processes had a slower rate than dry oxidation at 1050°C and below. The dry oxides exhibited a very flat surface; in contrast, SEM and TEM revealed that wet oxidation preferentially oxidizes dislocation bands, causing raised lines on the oxide and corresponding grooves in the SiC. It was proposed that the much higher solubility of H₂O in SiO₂ as compared to that of O₂ allows wet oxidation to be preferential.

All of the oxidation studies on all polytypes of semiconductor quality SiC have been conducted on n-type material with the exception of the investigation by Palmour *et al.* [6]. The objective of this study was the determination of the redistribution of the common electrical dopants of N, P, Al and B during thermal oxidation of SiC films at 1200°C in dry O₂. Experimental segregation coefficients and interfacial concentration ratios were determined. Secondary ion mass spectrometry revealed that B and Al depleted from the SiC into the growing oxide while N and P were found to pile up in the SiC as a result of the loss of the SiC to the oxide formation. Aluminum is now used almost universally as the p-type dopant in SiC. The electrical properties of oxides thermally grown on n-type SiC normally have reasonably favorable characteristics of high breakdown voltage and low leakage currents. However, the reverse is true for thermally grown oxides on p-type SiC, as shown by Baliga and his students at NCSU. It is believed that at least two of the causes of the poor performance on a p-type material are the existence of the Al in the oxide and at the oxide/SiC interface and the dangling oxygen bonds which this species creates in the oxide as a result of a difference in oxidation state (+3) compared to that of Si (+4) and the existence of C at the SiC/insulator interface. Methods of effectively cleaning SiC surfaces prior to oxidation to deposit and grow oxides on p-type material under UHV conditions and determine the effect of Al redistribution and C concentrations at the interface on the properties of the oxide must be determined. In addition,

the effect of existing line and planar defects in the SiC epi-layer on the properties of the thermally grown and deposited oxide must be ascertained.

The research conducted in this reporting period and described in the following sections has been concerned with (1) design of a new CVD SiC system for the deposition of SiC films, (2) simulations and initial measurements of the impact ionization coefficients of electrons and holes in SiC devices, (3) deposition, annealing and electrical characterization of Ni, NiAl and Au contacts to p-type SiC, (4) the design of an integrated cleaning and oxidation system and (5) the design of a mask set to fabricate metal oxide-semiconductor gated diodes as a test of the interface electrical properties between insulators and SiC. The following individual sections detail the procedures, results, discussions of these results, conclusions and plans for future research. Each subsection is self-contained with its own figures, tables and references.

References

1. M. Bhatnagar, Ph. D. Thesis, North Carolina State University, 1994.
2. D. Alok, B. J. Baliga and P. K. McLarty, IEDM Technical Digest, IEDM 1993, 691 (1993).
3. R. C. A. Harris and R. L. Call in *Silicon Carbide-1973*, R. C. Marshall, J. W. Faust and C. E. Ryan, Eds. University of South Carolina Press, Columbia, S. C., 1974, pp. 534.
4. Suzuki, *et al.*, Jap. Journ. Appl. Phys. **21**, 579 (1982).
5. B. E. Deal and A. S. Grove, J. Appl. Phys. **36**, 3770 (1965).
6. J. W. Palmour, R. F. Davis, H. S. Kong, S. F. Corcoran and D. P. Griffis, J. Electrochem. Soc. **136**, 502 (1989).

II. Design of Novel Chemical Vapor Deposition System for Growth of SiC Films

Work on the design and fabrication of a novel CVD system for SiC deposition is in the preliminary stages at this time. A review of articles detailing system construction and discussions regarding the science of SiC deposition and analysis are being reviewed. The effort in the next reporting period will be directed towards the production of engineering drawings, the placement of orders for the various parts and the construction and operation of this system.

III. Correlation of Breakdown Voltage and Leakage Currents with Defects and Impurities

A. Introduction

Silicon carbide has been projected to be an excellent semiconductor for high-power, high-frequency and high-temperature applications [1,2]. This is attributed to the high critical electric field strength of SiC. One of the important parameters of a power device is its breakdown voltage and it is essential to have an exact knowledge of the impact ionization coefficients in order to understand the breakdown characteristics of the semiconductor. In addition, commercialization of SiC-based power devices requires the understanding of the nature of the defects responsible for the degradation in the breakdown voltage and an observed increase in the leakage current. A correlation between the epitaxial growth conditions and electrically active defects remains to be established.

A scanning electron microscope (SEM) will be used as the primary tool for characterizing the electrically active defects in 6H and 4H-SiC epitaxial layers grown in the task and also for measuring the impact ionization coefficients in SiC. In the context of this research project, high spatial resolution of the SEM will allow impact ionization measurements to be performed at defect free regions, as well as at the defect locations, to quantify the degradation caused by the various defect structures. To our knowledge, this will be the first attempt to quantify the role of defects on impact ionization in semiconductor devices. The SEM will also be used for the measurements of lifetime and diffusion length in SiC [2,3].

B. Experimental Setup

A scanning electron microscope, in the EBIC mode, will be used primarily for the identification of the electrically active defects in the 4H and 6H SiC epitaxial layers grown in the task. The utility of the SEM is threefold:

1. The SEM can be used to perform measurements of impact ionization coefficients using a blanked electron beam. The experimental setup is shown in Fig. 1. The setup is used to generate the photocurrent vs. reverse bias voltage curve of a reverse biased Schottky barrier diode illuminated by a pulsed source, namely a blanked electron beam.

The sample is reverse biased and the current generated in the diode by the pulsed excitation is tracked using a lock-in amplifier which is referenced to the beam blanking unit. This current is measured as a voltage drop across a current sensing resistor (R_s) which is in series with the devices. The generated current (i.e. the photocurrent) is plotted as a function of the applied reverse bias and an IV curve is thus generated. The power supply and the lock-in amplifier is interfaced with the PC to enable reliable data acquisition and analysis. Labview software is being used to control the setup through the PC, as well as for data acquisition.

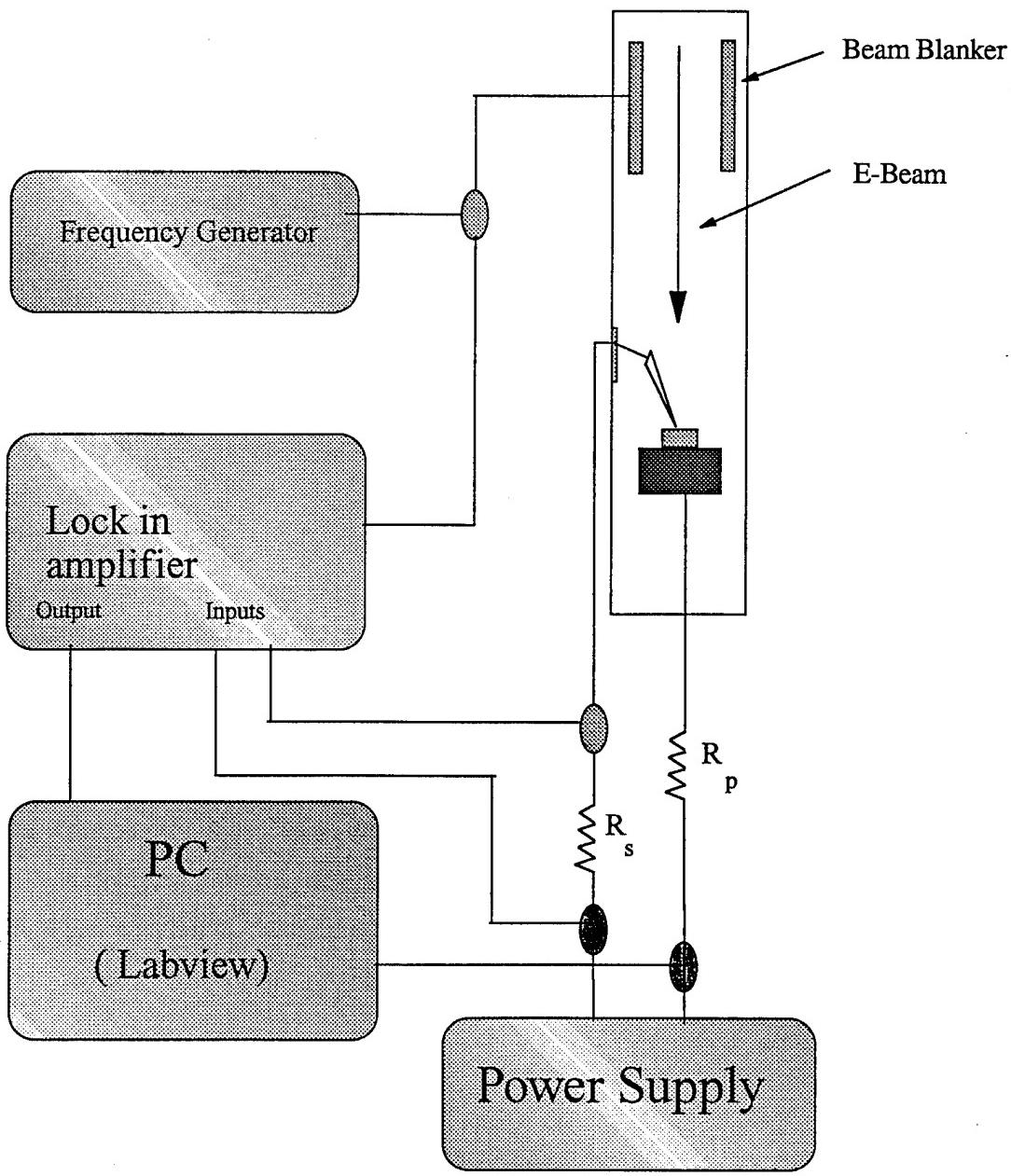


Figure 1. Experimental setup used.

Analytical expressions have been derived for the extraction of the impact ionization coefficients of electron and holes from the IV curve of a device with a constant electric field profile in its drift region. Simulations are being performed to obtain a structure with a constant electric field profile that would allow separation of the impact ionization of electrons and holes.

2. The SEM in the EBIC mode will be used for measuring the effect of the defects on the breakdown characteristics of the device. The EBIC allows the observation of the electrically active defects in the epitaxial layers in contrast to the metallurgical techniques that identify crystallographic defects. The EBIC allows depth resolution of the electrical activity by variation of the beam voltage. Variation of the bias on the diode will allow analysis of the electrical nature of the defect. At low reverse bias on the Schottky diode, the EBIC display will reveal defects that enhance recombination in the local regions. At high reverse biases on the Schottky diodes, EBIC reveal defects that enhance impact ionization. The electron energy will be varied to obtain a depth resolution of the defects.
3. The SEM with the beam blanking will also be used to measure the lifetime and diffusion length in SiC. A power supply (3KV) with a IEEE-488 interface was obtained from Bertan Associates, Inc. Both the power supply and the lock-in-amplifier have IEEE-488 interface to facilitate data acquisition and analysis through the PC. Work is now progressing to automate the setup and interface the equipment with the PC.

C. Results

A Hitachi scanning electron microscope was ordered and since delivery, work has occurred on the experimental setup and on obtaining the device configuration that would allow extraction of the parameters. The probes needed special design consideration, as they had to be able to withstand high voltages of up to 2000V. The probes and power supply were ordered and obtained.

Analytical expressions were derived for the extraction of impact ionization coefficients from the I-V curve of a given diode for a constant electric field profile in the drift region. The expressions are as follows:

$$1 - 1/M_p = (\alpha_p / (\alpha_n - \alpha_p)) [\exp(\alpha_n - \alpha_p) W - 1],$$

and

$$1 - 1/M_n = (\alpha_n / (\alpha_p - \alpha_n)) [\exp(\alpha_p - \alpha_n) W - 1].$$

When $\alpha_p \gg \alpha_n$, Eq. 1 reduces to

$$\alpha_p = [1n(M_p)] / W.$$

Similarly, when $\alpha_n \gg \alpha_p$, Eq. 2 reduces to

$$\alpha_n = [1n(M_n)] / W.$$

Extensive two-dimensional numerical simulations have been performed to formulate an extraction procedure for impact ionization coefficients of electrons and holes using a constant

electric field profile. In order to verify the extraction procedure, simulations were done for silicon so as to obtain the IV characteristics of a simple p-n junction diode with JTE termination. A junction depth of 20 microns and a low doping concentration of $1e14 \text{ cm}^{-3}$ was chosen for the epitaxial layers in order to obtain a fairly constant electric field profile. The implant dose for the JTE termination was optimized to a value of $2.6e12 \text{ cm}^{-2}$ in order to achieve a near ideal breakdown voltage. Simulations were performed with and without impact ionization and the impact ionization coefficients were extracted using the analytical expressions derived earlier. Agreement between the ionization coefficient that is input into the simulator, as a material parameter, and the impact ionization coefficient extracted using the analytical expression derived, indicated that the proposed extraction procedure was accurate. The device structure used for the extraction, the IV curve obtained from the simulation and the extracted ionization coefficients are shown in Fig. 2.

D. Discussion

As seen in Fig. 2, ionization coefficients extracted using the technique described earlier coincided well with the impact ionization coefficients of electrons that was input in the simulator. The reason being the impact ionization of electrons dominate that of the holes as a result of which the impact ionization due to holes is suppressed. Simulations are now being performed to obtain a device structure that would allow separation of the impact ionization due to electrons and holes and at the same time allow a constant electric field profile needed for the extraction to be obtained.

Preliminary impact ionization measurements have been performed using the setup described. Although this allowed the verification of the measurement procedure, accurate measurements were not possible because of equipment limitations. For this reason, it has been concluded that a dedicated SEM is required with computer-controlled measurements in order to obtain accurate data.

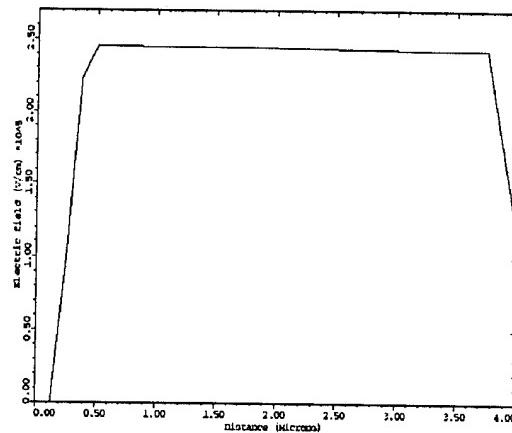
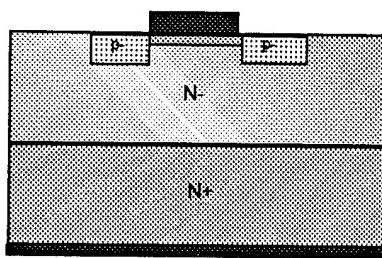
E. Conclusions

In conclusion, the experimental procedure for the extraction of the impact ionization co-efficients has been defined and set up. The experimental setup involves generating carriers in the depletion region by a pulsed source, namely a blanked electron beam, in a reverse biased junction. The generated carriers are tracked using a lock-in-amplifier that is referenced to the pulse generator of the beam blanking unit. The current is measured as a voltage drop across a resistor in series with the devices and an I-V curve is thus generated by plotting this current vs. the applied reverse bias. Analytical expressions have been derived for the extraction of impact ionization coefficients from the I-V data obtained. The validity of these expressions has been ascertained by comparing the extracted parameters, for a simple p-n junction diode with JTE

2a

2b

Device Structure



2c

2d

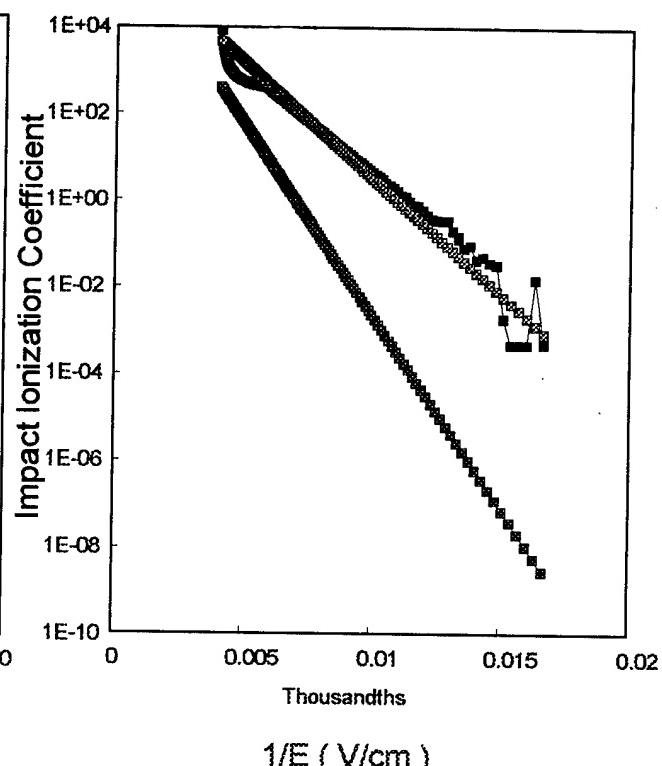
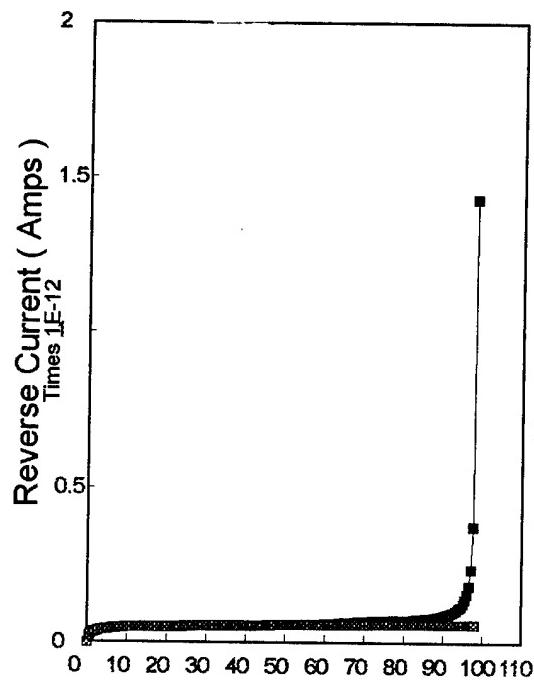


Figure 2. a) Device structure used in simulation. b) Electric field profile obtained from simulations. c) I-V characteristics of the device with and without impact ionizations. d) impact ionization coefficient extracted using the analytical solution developed.

termination, with the values of ionization coefficients input into the simulator as a material parameter. Impact ionization due to electrons was found to dominate the impact ionization due to holes, which tends to make the extraction of impact ionization coefficients due to holes very difficult.

F. Future Research Plans and Goals

Simulations will be performed in order to obtain device structure with a constant electric field profile that would allow separation of impact ionization of electrons and holes. The setup will be automated through the PC in order to facilitate accurate measurement and extraction. EBIC studies will be performed in order to study the nature of the electrical defects and their effect on the breakdown characteristics. EBIC studies will also be performed in order to measure lifetime and diffusion length in SiC.

G. References

1. B. J. Baliga, *Power Semiconductor Devices and Circuits*, Ed. by A. A. Jaecklin, Plenum Press, 377, 1992
2. M. Bhatnagar and B. J. Baliga, IEEE Transactions on Electron Devices **40** (3), 1993.
3. A. Boudjani, G. Bassou, T. Benbakhti, M. Beghdad and B. Belmekki, Solid State Electronics **38** (2), 471, 1995
4. V. K. S. Ong, J. C. H. Phang and D. S. H. Chan, Solid State Electronics, **37** (1), 1, 1994.

IV. Development of a System for Integrated Surface Cleaning and Oxide Formation on 6H-SiC

A. Introduction

The development of high-temperature, -power and -frequency devices based on SiC requires a complete understanding of the oxide formation and interface characteristics. By using an integrated UHV system that contains remote plasma cleaning, HF vapor phase oxide removal, and various oxide deposition capabilities, interfaces with lower contaminant levels will be prepared while a better understanding of the SiC oxide formation process is gained. The UHV compatible cleaning and oxide formation system will be integrated with an advanced system that includes other processing and characterization capabilities. The UHV surface characterization system will allow for *in vacuo* characterization of the SiO₂/SiC interface and oxides grown by various individual and combination processes.

B. Experimental Procedure

The integrated system will allow for most of the characterization to be accomplished without exposing samples to the ambient. Furthermore, the processes will be characterized at various stages in the process, thus allowing for the understanding of the entire oxidation process. A typical process is given as follows:

1. the native oxide is removed via the HF vapor system,
2. the sample is cleaned using a hydrogen plasma,
3. the sample is characterized using the various systems available: Raman Spectroscopy, UV Photoemission, LEED/Auger, UPS, and XPS,
4. the oxide layer is deposited using a combination of thermal or plasma CVD.

The H-plasma step removes any residual contaminants left after the HF cleaning and results in a H-terminated surface and then characterizes the various grown oxide layers in order to determine the characteristics of the different growing techniques.

The unique capability that will be employed in this study is an integrated processing system with *in situ* diagnostics. The system is shown schematically in Fig. 1. The system includes advanced surface characterization, surface preparation, and growth capabilities. Included in this proposal is the development of a UHV CVD/oxidation system which would be constructed to be compatible with the integrated system. The system is based on a UHV linear sample transfer mechanism. This transfer chamber is 35 feet long and connects eight separate surface preparation, processing or characterization chambers. Techniques relevant to this study include the remote plasma surface preparation chamber, LEED, AES, XPS, uv-photoemission, thermal desorption, and AlN deposition. Other chambers which could prove useful include *in situ* Raman spectroscopy and Si MBE.

INTEGRATED GROWTH/CHARACTERIZATION SYSTEM

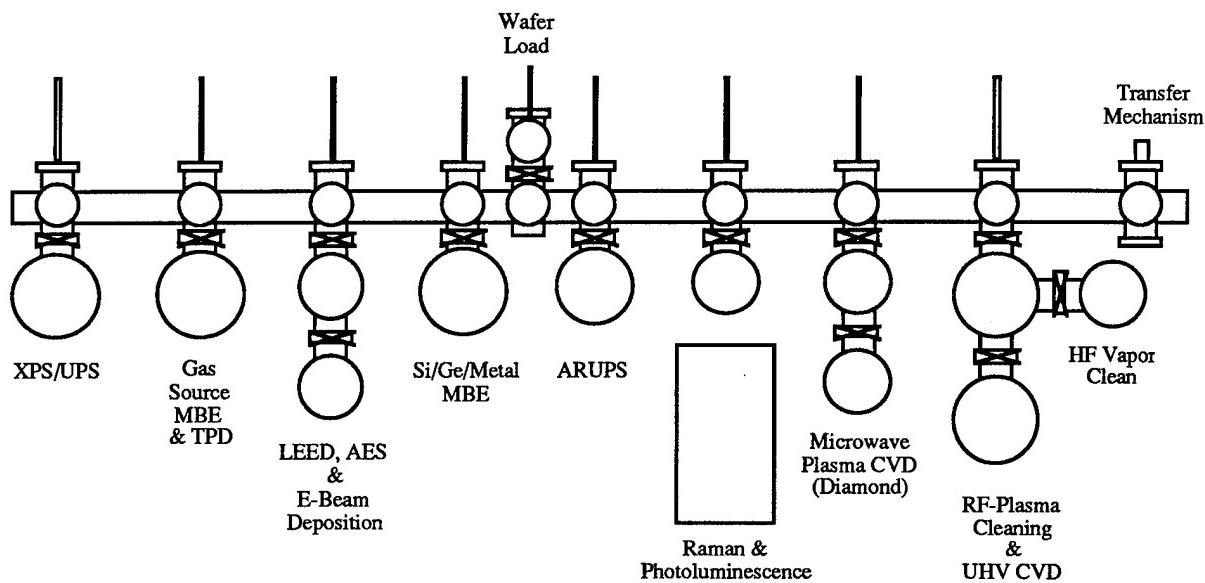


Figure 1. Schematic of the integrated growth and characterization system to be employed in the studies of defects in insulators on SiC.

C. Conclusions

The integrated UHV system will be able to explore processes that have previously been unobtainable. The uniqueness of the cleaning system integrated with the growth and characterization system allows for capabilities that have not been previously used in the characterization and growth of oxides on SiC.

D. Future Research Plans and Goals

There will be considerable focus on the examination of the oxide layers for use as gate insulators in field effect devices. A process by which the gate oxide and gate can be applied to an industrial setting will be attempted.

V. Characterization of Oxides on N- and P-type 4H- and 6H-Silicon Carbide

A. Introduction

Silicon carbide (SiC) has been shown to be an excellent material for the fabrication of devices for high-power, high-frequency and high-temperature applications [1]. The advantages of SiC metal oxide semiconductor field effect transistors (MOSFETs) has also been discussed [2]. The successful operation of these devices hinges on the interface and bulk properties of the gate dielectric, usually an oxide. Previous researchers have reported results on thermally grown oxides on N-type [3-6] and P-type 6H-SiC [5,7-11]. While the results obtained on N-type 6H-SiC have shown that those oxides are of high quality, oxides grown on P-type 6H-SiC exhibit large flatband voltage shifts and are, thus, unsatisfactory for application as gate dielectrics. Oxides deposited under special conditions with surface preparation specific to the particular deposition might show improved interfacial properties over thermally grown oxides.

The SiO_2 -SiC interfaces will be characterized using capacitance-voltage (C-V) measurements [12]. A Mask set has been designed to fabricate the MOS structures required for accurate and complete electrical characterization. It is proposed to study the properties of thermally grown oxides on 6H-SiC and 4H-SiC until it is possible to obtain wafers with oxides deposited by Prof. Nemanich's group with the specific pre-deposition surface treatments and deposition conditions.

B. Experimental Procedure

Thermally grown (dry) oxides on both N-type and P-type 6H-SiC have been characterized in our group [4,8]. It is planned to use thermal oxides grown under conditions identical to those used in the previous work. The procedure for the thermal oxidation followed during the previous work is described next. The results obtained during the study will also be briefly discussed.

The wafers were first subjected to a pre-oxidation RCA clean. The wafers were then oxidized in dry oxygen at 1275°C for 45 minutes. The push-pull times were 5 minutes and the furnace ramp-up and ramp-down rates were $15^\circ\text{C}/\text{min}$ and $5^\circ\text{C}/\text{min}$ respectively. The oxide thickness was ellipsometrically measured to be about 550\AA . Aluminum dots were then evaporated onto the oxide films using a shadow mask. A large area blanket evaporation of aluminum was also done on the backsides of these wafers to provide a large area ohmic contact. Electrical characterization of the oxide films was done with C-V and current-voltage (I-V) measurements.

C-V curves obtained from MOS capacitors fabricated on the thermally grown oxide on N-type 6H-SiC showed distinct regions of accumulation, depletion and deep depletion. Inversion was not observed as the measurements were made in the dark at room temperature

and since the generation of minority carriers is extremely slow in SiC due to its wide bandgap. A low effective oxide charge density of $1 \times 10^{11} \text{ cm}^{-2}$ was determined from the flatband voltage shifts measured from the C-V curves. An artificially low interface state density at mid-gap of $5 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ was also measured. This value is much lower than the actual D_{it} at mid-gap since the interface states deep in the band-gap are not in equilibrium with the Fermi level due to the extremely slow capture rates at room temperature. I-V measurements on these oxide films showed that the current conduction followed the Fowler-Nordheim mechanism. A barrier height of 2.7eV between the SiC and the oxide was calculated and the electron affinity of 6H-SiC was determined to be between 3.7 and 3.8eV. The breakdown electric field strength measured for these oxide films was 10MV/cm which is comparable to that obtained on oxides grown on silicon. In summary, thermally grown oxides on N-type 6H-SiC were shown to be of high quality and comparable to thermal oxides grown on silicon.

Distinct regions of accumulation, depletion and deep depletion were observed in C-V curves on MOS capacitors fabricated on thermally grown oxide on P-type 6H-SiC. A large flatband voltage shift was observed in the C-V curves and a large effective charge density of $8 \times 10^{12} \text{ cm}^{-2}$ was calculated from the flatband voltage shift. An interface state density of $1 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ was also measured. Bias Temperature Stress measurements were done to determine the nature of the charges present in the oxides. Negative Bias Stress Instability was observed in the oxide when the negative stress of -50 IV was applied for 30 minutes with the capacitor at 200°C as the stress induced the creation of fixed charges in the oxide and some slow trapping in the oxide, as well. I-V measurements on these capacitors showed a weak dependence on temperature and it was concluded that the current mechanism was not of the Frenckel-Poole type. The large effective oxide charge prevented an accurate estimation of the electric field in the oxide. The conclusion drawn from this study was that large positive effective charge is present in these oxides and the dry oxide grown on P-type 6H-SiC is not superior to wet oxide grown on P-type 6H-SiC at lower temperatures. It was also concluded that the oxide would be unsuitable as a gate dielectric for MOSFETs.

C. Results

The proposed process to fabricate the MOS capacitors and the gated diodes is described in this section. The wafer is subjected to a sacrificial oxidation to clean the surface. A low temperature oxide (LTO) of thickness 6000Å is deposited on the wafer. This oxide is then patterned so that the regions to receive the N⁺ implant are exposed. Another layer of LTO of thickness 1000Å is deposited on the wafer. This 1000Å of oxide acts as a pad oxide during the implant step. The patterned wafer is subjected to a nitrogen implant to form the N⁺ highly doped regions. The wafer is then subjected to a high temperature anneal to activate the dopant. The oxide is further patterned to define the gate region and the gate dielectric thermally grown

or deposited on the SiC. A blanket deposition of polysilicon is then done and is heavily doped N^+ *in situ* with $POCl_3$. The poly is then patterned to form the gate. Using the poly as a mask, the gate dielectric not covered by the poly is etched off. Ti/Al is then deposited and patterned by lift-off to form the metal contacts to the poly and the N^+ source. A large area backside blanket evaporation of Al is done to form an ohmic contact. The final structure of the MOS capacitors and the gated diodes is shown in Figs. 1 and 2.

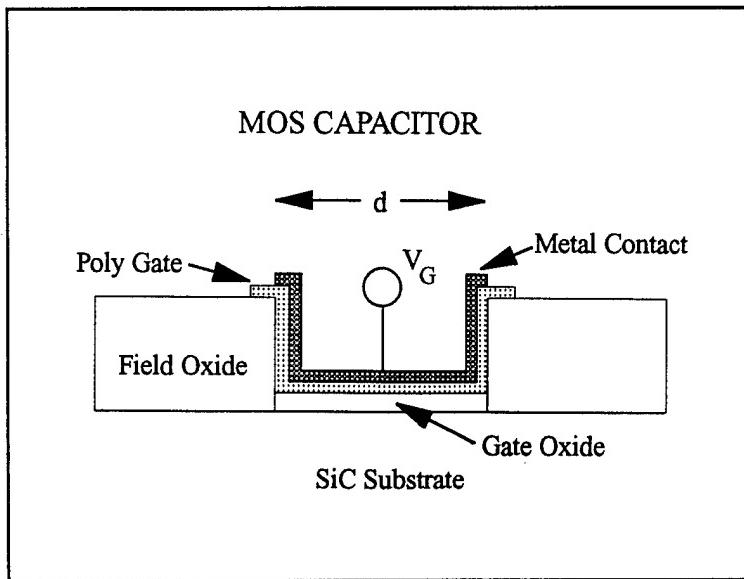


Figure 1. Poly-gated MOS capacitor with Ti/Al metal contact. Substrate contact from backside of wafer. Diameter of capacitor = 50,100,300 μm .

C. Discussion

Several previous workers have discussed the problems of using MOS capacitors in the characterization of the SiO_2/SiC interface [6,9-11]. The wide band-gap of SiC means the generation rate of minority carriers inside the depletion region is very slow and the concentration of minority carriers in the bulk of the SiC is also very low. As a result, interface states deep in the band-gap capture minority carriers extremely slowly, even when the position of the Fermi level inclines the state to be occupied by the minority carrier. Therefore, conventional high-low CV measurements made at room temperature in the dark on MOS capacitors yield accurate information on D_{it} only very close to the majority carrier band. This phenomenon is analogous to that already observed on silicon MOS capacitors at 77K [13].

To obtain information on the interface closer to midgap, the capture rates of minority carriers by the deep interface states must be enhanced by increasing the concentration of minority carriers in the depletion region. This can be achieved by elevating the

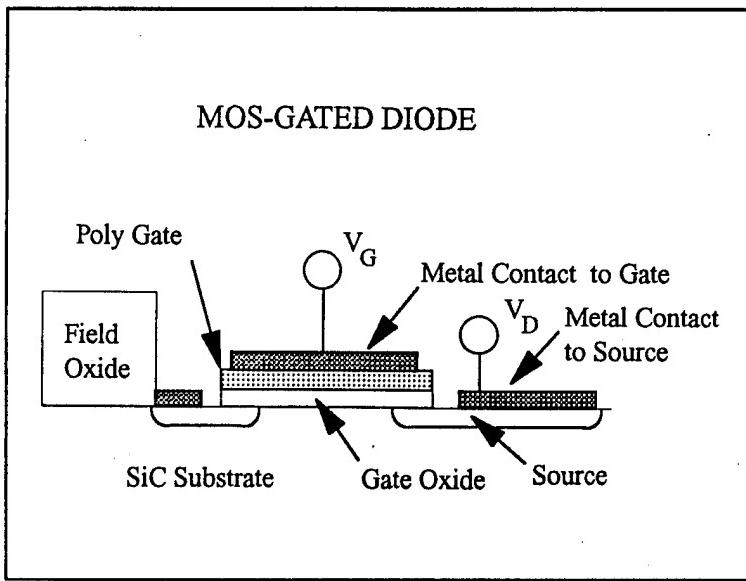


Figure 2. MOS-gated diode with separate Ti/Al contacts to poly gate and N+ source. Diameter of gate = 300 μm . Substrate contact from backside of wafer.

measurement temperature which increases the thermal generation rate of minority carriers in the depletion region below the gate, or by using photogeneration which excites minority carriers in the depletion region, or by using a P-N junction to inject the minority carriers under the gate. Since the main applications of the MOS structure would be in devices which have P-N junctions to inject minority carriers (relative to the substrate) below the gate, the use of the such a structure (the gated diode) in the measurement would not only yield more accurate information about the interface than the use of a simple MOS capacitor but would also give an idea of the performance of the MOS structure under conditions that it would be subjected to in inversion-layer devices such as MOSFETs. Keeping this in mind, the Mask set has been designed to fabricate gated diodes and MOS capacitors of different gate areas to study the interface.

E. Conclusions

A Mask set has been designed to fabricate devices that would enable accurate characterization of the SiO_2 -SiC interface. Devices that will be fabricated include MOS capacitors and MOS gated diodes. The wide band-gap of SiC and the attendant modifications this fact introduces in the characterization of the interface as opposed to the characterization of the SiO_2 -Si interface have been recognized. We are ready to place an order for the fabrication of the Mask set.

F. Future Research Plans and Goals

The Mask set designed for the fabrication of devices used in the characterization will be ordered. Once the Mask set has arrived, devices will be fabricated on thermal oxide using an already developed process and the SiO₂-SiC interface will be characterized.

G. References

1. R. J. Trew, J.-B. Yan and P. M. Mock, Proc. IEEE **79**, 598 (1991).
2. M. Bhatnagar and B.J. Baliga, IEEE Trans. on Electron Devices **40**, 645 (1993).
3. A. Suzuki, H. Ashida, N. Furui, K. Mameno and H. Matsunarni, Jpn. J. of Applied Physics **21**, 579 (1982).
4. Dev Alok, P.K. McLarty and B.J. Baliga, Applied Phys. Lett. **64**, 2845 (1994)
5. T. Ouisse, N. Becourt, C. Jaussaud and F. Templier, J. of Applied Physics **75**, 604, (1994).
6. P. Neudeck, S. Kang, J. Petit, and M. Tabib-Azar, J. of Applied Physics **75**, 7949 (1994).
7. C. Raynaud, J.-L. Autran, B. Balland, G. Guillot, C. Jaussaud and T. Billon, J. of Applied Physics **76**, 993 (1994).
8. Dev Alok, P. K. McLarty, and B. J Baliga, Applied Phys. Lett. **65**, 2177 (1994).
9. J.N. Shenoy, G.L. Chindalore, M.R. Melloch, J.A. Cooper Jr., J.W. Palmour and K.G. Irvine, Journal of Electronic Materials **24**, 303 (1995).
10. J. N. Shenoy, L. A. Lipkin, G. L. Chindalore, J. Pan, J. A. Cooper Jr., J. W. Palmour and M. R. Melloch, *Proc. 21st Intl. Symp. on Compound Semiconductors*, 499, San Diego (1994).
11. S. T. Sheppard, M. R. Melloch and J. A. Cooper Jr., IEEE Trans. on Electron Devices **41**, 1257 (1994).
12. E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Wiley (1991).
13. A. Goetzberger and J. C. Irvin, IEEE Trans. on Electron Devices **15**, 1009, (1968).

VI. Rectifying and Ohmic Contacts for P-type Alpha (6H) Silicon Carbide

A. Introduction

The formation of low resistivity and thermally stable ohmic contacts to 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have the advantage over Si, the contact resistivities must be below $1 \times 10^{-5} \Omega \text{-cm}^2$ [1]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on Al or Al alloys to dope the SiC surface below the contacts. While the fabrication of ohmic contacts to SiC also has usually depended on very heavily-doped surfaces, the introduction of high levels of dopants in the near surface device region of the epilayer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice. Based on all of these issues and experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

Low resistance contacts to p-type SiC remain a substantial challenge for high temperature and high-power devices. An Al-Ti alloy [2] annealed at 1000°C for 5 min. was reported to yield contact resistances ranging from $2.9 \times 10^{-2} \Omega \text{ cm}^2$ for a carrier concentration of $5 \times 10^{15} \text{ cm}^{-3}$ to $1.5 \times 10^{-5} \Omega \text{ cm}^2$ for $2 \times 10^{19} \text{ cm}^{-3}$. The thermal stability of these contacts was not reported. Aluminum deposited on a heavily-doped 3C-SiC interlayer on a 6H-SiC substrate and subsequently annealed at 950°C for 2 min. reportedly yielded contact resistivities of $2-3 \times 10^{-5} \Omega \text{ cm}^2$ [3]. Because of its low melting point (660°C), however, pure Al would be unsuitable for high temperature applications. Platinum contacts annealed from 450 to 750°C in 100°C increments were also used as ohmic contacts to p-type SiC [4]. These contacts, which rely on the combination of a highly-doped surface and the high work function of Pt, have not been known to yield contact resistivities as low as those for the contacts containing Al.

Because Ni forms stable silicides but not carbides, it has the potential to draw Si out of the lattice, allowing Al to diffuse into the SiC and occupy Si sites. In contrast, Ti forms a very stable carbide [5] in addition to silicides and, therefore, readily competes for the C in TiAl contacts. This report describes electrical characteristics and chemical profile results of as-deposited NiAl Schottky contacts and NiAl ohmic contacts annealed at 1000 °C (10 to 80 s) on p-type 6H-SiC (0001). Future experiments with these contacts are also discussed along with other contact schemes which do not incorporate Al.

B. Experimental Procedure

Vicinal, single-crystal 6H-SiC (0001) wafers provided by Cree Research, Inc. were used as substrates in the present research. The wafers were doped with N or Al during growth to create n- or p-type material, respectively, with carrier concentrations of $1\text{--}5\times10^{18}\text{ cm}^{-3}$. Homoepitaxial layers (1–5 μm thick) grown by chemical vapor deposition (CVD) were Al-doped with carrier concentrations ranging from 1×10^{16} to $1\times10^{19}\text{ cm}^{-3}$. The surfaces were oxidized to a thickness of 500–1000 \AA in dry oxygen. The substrates were simultaneously cleaned and the oxide layer etched from the surface using a 10 min. dip in 10% hydrofluoric acid, transferred into the vacuum system, and thermally desorbed at 700 °C for 15 min. to remove any residual hydrocarbon contamination.

A UHV electron beam evaporation system was used to deposit the NiAl and Ni films. After depositing 1000 \AA of NiAl, 500–1000 \AA of Ni was deposited as a passivating layer. Pure Ni (99.99%) and pure Al (99.999%) pellets were arc melted to form alloyed pellets of 50:50 atomic concentration for evaporation of NiAl. The films were deposited onto unheated substrates at a rate of 10–20 $\text{\AA}/\text{s}$. The pressure during the depositions was between 5×10^{-9} and $5\times10^{-8}\text{ Torr}$.

Circular contacts of 500 μm diameter were fabricated for electrical characterization by depositing the metal films through a Mo mask in contact with the substrate. Silver paste served as the large area back contact. For contact resistance measurements, TLM patterns [6] were fabricated by photolithography. The Ni/NiAl films were etched in phosphoric acid : acetic acid : nitric acid (12 : 2 : 3) at 50 °C (etch rate $\approx 30\text{ \AA}/\text{s}$). The contact pads were $300\times60\text{ }\mu\text{m}$ with spacings of 5, 10, 20, 30 and 50 μm . Mesas in the substrate were not fabricated. All subsequent annealing was conducted in a N_2 ambient in a rapid annealing furnace.

Electrical characteristics were obtained from current-voltage and capacitance-voltage measurements. Current-voltage (I-V) measurements were obtained with a Rucker & Kolls Model 260 probe station in tandem with an HP 4145A Semiconductor Parameter Analyzer. Capacitance-voltage (C-V) measurements were taken with a Keithley 590 CV Analyzer using a measurement frequency of 1 MHz.

Auger electron spectroscopy (AES) was performed with a JEOL JAMP-30 scanning Auger microprobe. The films were sputtered with Ar ions at a beam current and voltage of 0.3 μA and 3 kV, respectively, to obtain composition profiles through the thickness of the films.

C. Results

Chemical Characterization of As-deposited Films. The composition of the NiAl films deposited at room temperature were analyzed with AES. The first films deposited were found to contain approximately 3 at. % O. This contamination was attributed to O found in the Ni source. Alloyed pellets were subsequently fabricated using a new Ni source (99.99%).

An Auger depth profile of a film deposited from the latter source is shown in Fig. 1. While there was some modulation of the intensities, the overall composition remained relatively stable. The relative intensities of Ni and Al calculated from pure Ni and pure Al standards and their corresponding sensitivity factors are shown in Fig. 2. The average atomic composition was approximately 50:50.

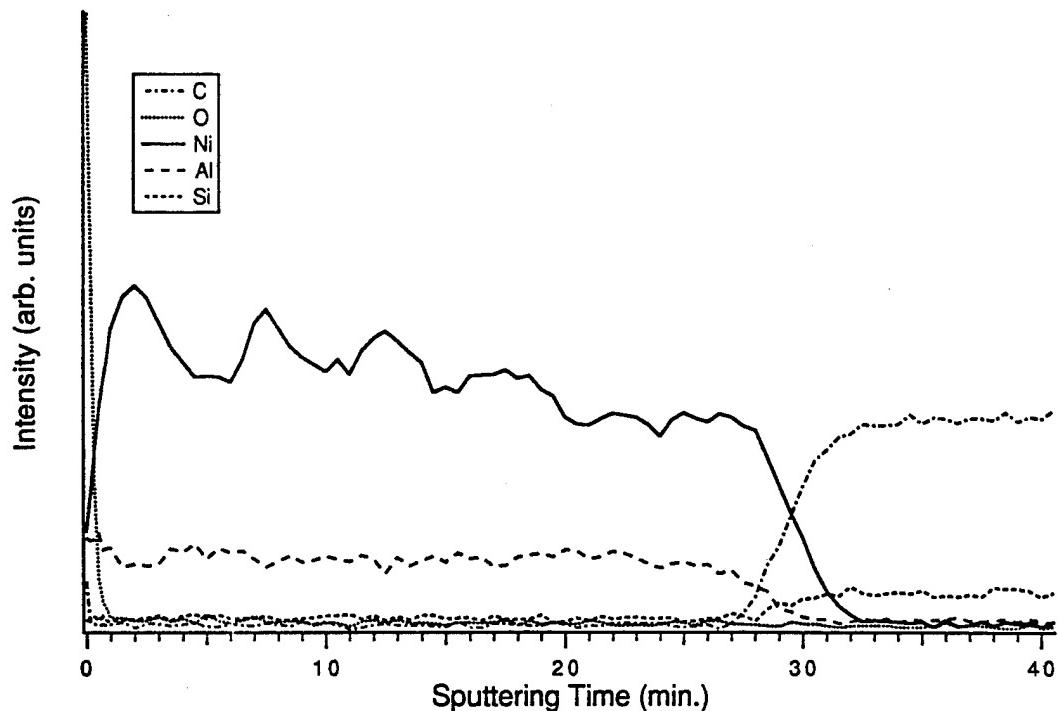


Figure 1. AES composition profile of 1000 Å of NiAl deposited at room temperature on (0001) 6H-SiC.

Schottky Contacts. In the as-deposited condition the Ni/NiAl contacts were rectifying on p-type SiC with carrier concentrations of 1.6×10^{16} and $3.8 \times 10^{18} \text{ cm}^{-3}$ in the epilayer. The sample with the lower carrier concentration displayed leakage current densities of $\sim 1 \times 10^{-8} \text{ A/cm}^2$ at 10 V and ideality factors between 1.4 and 2.4, while the latter sample displayed approximately five orders of magnitude higher leakage current densities and similar ideality factors. The average Schottky barrier heights (SBH's) calculated for the samples with the lower and higher carrier concentrations were 1.37 and 1.26 eV, respectively. The lower SBH calculated for the former sample is likely due to enhanced thermionic field emission through the upper energy region of the barrier because of the narrower depletion region. Hence, the 1.37 eV value is believed to be more accurate.

Similar results were obtained for as-deposited Ni and Au contacts on p-type ($2.1\text{--}4.5 \times 10^{16} \text{ cm}^{-3}$) 6H-SiC (0001). These samples displayed similar leakage currents and

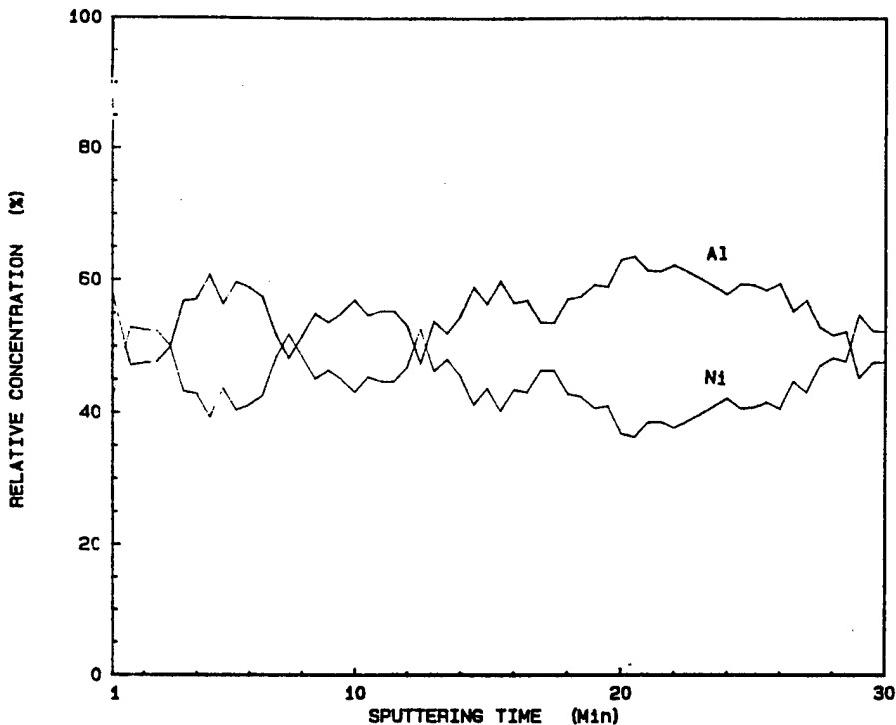


Figure 2. Relative concentrations of Ni and Al in the film represented in Fig. 1. The calculations were based on the signals from pure Ni and pure Al and their corresponding sensitivity factors.

ideality factors of 1.3–2.1 and <1.1, respectively. From these measurements SBH's of 1.31 eV for the Ni contacts and 1.27 eV for the Au contacts were calculated. In comparison, as-deposited Ni on n-type ($4.1 \times 10^{16} \text{ cm}^{-3}$) 6H-SiC (0001) yielded ideality factors below 1.1, similar leakage current densities to those stated above, and SBH's of 1.14 eV and 1.21 eV calculated from I-V and C-V measurements, respectively.

Our measurements on p-type SiC have shown consistent differences from measurements on n-type 6H-SiC. The SBH's tended to be higher on p-type than on n-type material. While leakage currents for Au, NiAl, and Ni contacts on p-type 6H-SiC were comparable to Ni contacts on n-type 6H-SiC, the ideality factors were higher on p-type SiC. The higher ideality factors for contacts on p-type SiC indicate that thermionic emission was not the dominant current transport mechanism. In the future we may investigate these contacts with deep level transient spectroscopy (DLTS) to determine whether recombination at deep levels accounts for the different electrical behavior of the contacts on p-type material.

Ohmic Contacts. The Ni/NiAl contacts were sequentially annealed for total times of 10–80 s at 1000 °C in a N₂ ambient. This temperature was used because (1) limited intermixing of Al and SiC was reported at 900 °C [7] and (2) other papers report annealing in this temperature range for Al-based ohmic contacts on p-type SiC [2, 3, 8]. Because of the

extremely high thermodynamic driving force for Al to form an insulating oxide layer (ΔG_f (Al₂O₃) ~ -1300 kJ/mol at 1000 °C [JANAF - Chase, M., et al., JANAF Thermochem. Tables, 3d Ed. J. Phys. Chem. Ref. Data, 1985. 14(Supp. 1)]), 1000 Å of Ni was deposited on top of the NiAl contacts to slow the oxidation process.

Table I summarizes the results of I-V measurements taken at selected intervals through the annealing series for three samples with various carrier concentrations in the SiC epitaxial layer (1.4×10^{18} , 5.7×10^{18} , and 1.5×10^{19} cm⁻³). The two samples with the lower carrier concentrations were not truly ohmic but became ohmic-like after annealing for 80 s. This annealing series will be continued to determine whether ohmic behavior in these two samples will ensue; however, the additional force on the probes needed to obtain consistent results indicates that an oxide has begun to form at the surface and may cause problems with further annealing. The sample with the higher carrier concentration was ohmic after annealing for 10 s. The calculated specific contact resistivity remained approximately 2.0×10^{-2} Ω cm² through annealing for 60 s. A slight increase to 3.1×10^{-2} Ω cm² was calculated after annealing for 80 s. This increase is believed to be due to the surface oxide layer.

Table I. Estimated specific contact resistivities / electrical behavior of Ni (1000 Å) / NiAl (1000 Å) / p-SiC after annealing at 1000 °C for 20, 40, 60, and 80 s for three samples with the carrier concentrations indicated. The specific contact resistivities were calculated from non-mesa etched linear TLM patterns.

Annealing Time	20 s	40 s	60 s	80 s
1.4×10^{18} cm ⁻³	non-ohmic	non-ohmic	non-ohmic	almost ohmic
5.7×10^{18} cm ⁻³	non-ohmic	non-ohmic	non-ohmic	almost ohmic
1.5×10^{19} cm ⁻³	2.0×10^{-2} W cm ²	1.9×10^{-2} W cm ²	2.2×10^{-2} W cm ²	3.1×10^{-2} W cm ²

The high contact resistivities may be a result of a few causes. It is believed that the SiC may be depleted of carriers near the surface, possibly due to thermal oxidation. A depletion of carriers near the surface would result in higher than expected contact resistivity values because current transport across the contact depends on the carrier concentration in the SiC at the SiC surface. To investigate this potential problem we plan to compare the contacts described above with contacts on SiC implanted with Al and also on SiC which has not been thermally oxidized. The values of specific contact resistivity stated above should only be considered as preliminary estimates since only one level of the TLM measurement pattern was used. In the near future we plan to employ a circular TLM measurement structure [9], which consists of only one level and does not involve etching of the substrate.

D. Discussion

An Auger depth profile (Fig. 3) of Ni/NiAl/SiC annealed at 1000 °C for 80 s shows that the surface oxide is thicker than that on the as-deposited sample (Fig. 1). After sputtering for a couple of minutes, the O concentration dropped to below detectable limits; however, the data shows a decreasing Al concentration in the direction toward the SiC interface. This indicates that the kinetics are more favorable for the Al to diffuse toward the surface and react with O than for the Al to react with the SiC. Some of the Ni has probably reacted with Si at the interface to form a silicide, as indicated by the local maximum in the Ni intensity near the SiC interface, while the peak in the C intensity indicates the presence of an adjacent C-rich layer.

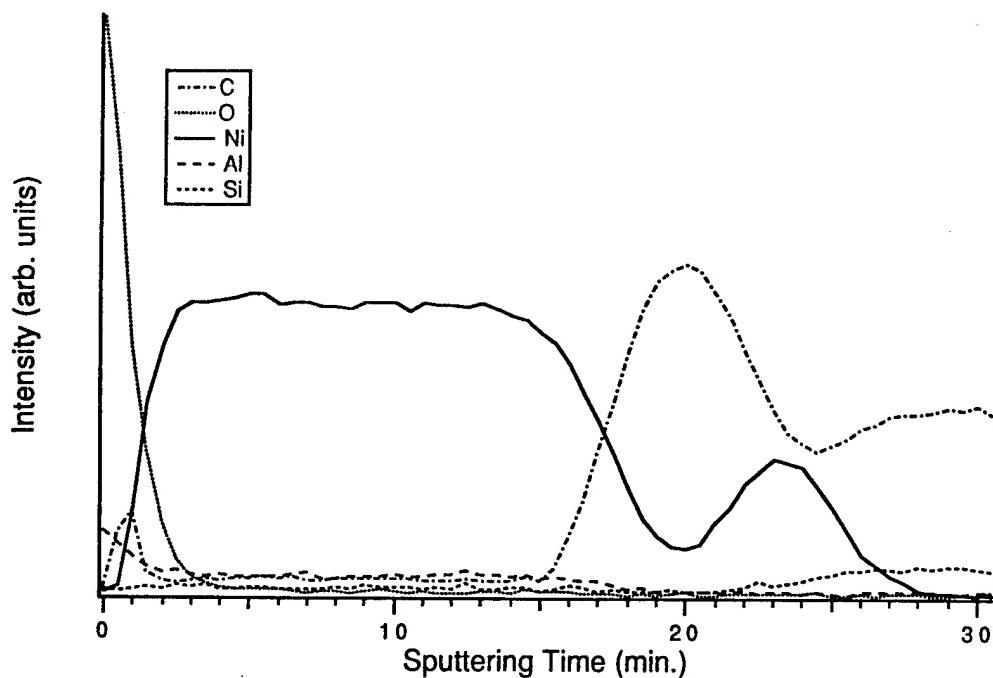


Figure 3. AES composition profile of Ni (1000 Å) / NiAl (1000 Å) / 6H-SiC annealed at 1000 °C for 80 s in N₂.

The demonstrated oxidation problem with Al necessitates the development of ohmic contacts which do not consist of substantial concentrations of Al. The following section discusses future plans for finishing the experiments on NiAl contacts and for initiating experiments on novel contact materials.

E. Conclusions

Nickel-aluminum was investigated primarily as an ohmic contact for p-type 6H-SiC because of the p-type doping of Al in SiC, the high melting point of NiAl (as compared to Al),

and the tendency of Ni to form silicides but not carbides. This latter property potentially could have resulted in extraction of Si from the SiC lattice in exchange for Al, thereby enhancing the p-type carrier concentration at the surface. Although the I-V measurements indicate that some Al may be diffusing into the SiC after the longest annealing time performed (80 s at 1000 °C), this potential for reaction between Al and SiC appears to be exceeded by the driving force for Al to diffuse to the surface and react with O. A concentration profile obtained from AES analysis shows that Al has diffused through the 1000 Å Ni overlayer to form a thin (200 Å estimated) oxide layer.

In addition to the ohmic behavior resulting from annealing the NiAl contacts, as-deposited Ni, NiAl, and Au contacts deposited at room temperature on p-type ($N_A < 5 \times 10^{16} \text{ cm}^{-3}$) 6H-SiC (0001) were rectifying with low leakage currents, ideality factors between 1.3 and 2.4, and SBH's of 1.31, 1.27, and 1.37 eV, respectively. These SBH's are higher than typically calculated for contacts on n-type 6H-SiC, as represented by the 1.14 eV value for Ni on n-type 6H-SiC and calculated from I-V measurements. A technique such as DLTS may be used to explain the different behavior between Schottky contacts on n- and p-type SiC.

F. Future Research Plans and Goals

To extend our study on NiAl ohmic contacts for p-type SiC, the contact resistivities for annealing series at 1000 °C will be repeated using circular TLM patterns and two different substrates: 1) SiC implanted with Al to increase the surface carrier concentration and 2) SiC which has not been thermally oxidized to investigate whether the bulk carrier concentration can be maintained at the surface. A photolithography mask with the circular TLM patterns was recently designed and will be used in our research on ohmic contacts in the very near future.

One alternate planned approach to Al-based ohmic contacts for p-type SiC will incorporate p-type semiconducting interlayers. The goal of this approach is to find a semiconducting material with a favorable band lineup with SiC (i.e., reduce the band bending) and to which an ohmic contact can easily be made. We have chosen to examine the $\text{In}_x\text{Ga}_{1-x}\text{N}$ system for interlayer materials because of the lower density of surface states (and hence less band bending) and the range of band gaps over the composition range. We plan to measure the valence band offsets and electrical characteristics between various compositions of $\text{In}_x\text{Ga}_{1-x}\text{N}$ (starting with $x=0$) and SiC. If a low energy barrier at the interface results, metals will be investigated for ohmic contacts for the interlayer / SiC structure.

The second approach involves using B-based contacts as an alternative to Al-based contacts. The main reasons for choosing B are that it is also a p-type dopant in SiC, its oxide is not as tenacious, and it is a much faster diffusant in SiC. Table II compares some important properties of B, Al, and their associated oxides. Although the B acceptor level in 6H-SiC is substantially deeper than that of Al, the fact that B is an acceptor makes it worth investigating

as a component in p-type ohmic contacts. As shown in Table II, the diffusion coefficient of B is at least three orders of magnitude greater than that of Al. Therefore, more B than Al will diffuse into the SiC at lower temperatures. As discussed in this report, a major problem with Al-based contacts is the strong driving force for forming an insulating oxide layer. This situation is shown by the extremely low equilibrium partial pressure, p_{O_2} , of O_2 for Al_2O_3 formation. While B_2O_3 also has a low p_{O_2} , it is significantly higher than that for Al_2O_3 , indicating that the driving force for B to form an oxide is significantly lower. In addition, the melting point of boron oxide is notably low.

Table II. Selected Properties of B, Al, and Their Associated Oxides.

Element	Activation Energy in 6H-SiC (meV)	Solid Source Diffusion, D_{SiC} @ 1800°C (cm ² /s)	Equilibrium partial pressure of O_2 , p_{O_2} @ 700°C (torr)	Melting temp. of the associated oxide, T_{melt} (°C)
B	700	10^{-11} [10-11]	10^{-35}	450
Al	240	$<10^{-14}$ [12]	10^{-47}	2040

We have chosen to investigate B_4C as a potential B-based ohmic contact to p-type 6H-SiC. This material was chosen because of its extremely low resistivity ($\rho < 1 \mu\Omega$ cm at R.T.), which is less than that of Cu ($\rho = 1.7 \mu\Omega$ cm at R.T.); its high melting point (2450°C); and its relatively small chemical potential gradient with SiC. These contacts will be deposited by ion beam assisted electron beam evaporation and/or sputtering.

G. References

1. D. Alok, B. J. Baliga, and P. K. McLarty, IEDM Technical Digest **IEDM 1993**, 691 (1993).
2. J. Crofton, P. A. Barnes, J. R. Williams, and J. A. Edmond, Appl. Phys. Lett. **62**(4), 384 (1993).
3. V. A. Dmitriev, K. Irvine, and M. Spencer, Appl. Phys. Lett. **64**(3), 318 (1994).
4. R. C. Glass, J. W. Palmour, R. F. Davis and L. S. Porter, U.S Patent No. 5,323,022 (1994).
5. J. L. Murray, Ed. *Phase Diagrams of Binary Titanium Alloys* (ASM International, Metals Park, Ohio, 1987).
6. H. H. Berger, Solid State Electronics **15**(2), 145 (1972).
7. V. M. Bermudez, J. Appl. Phys. **63**(10), 4951 (1988).
8. T. Nakata, K. Koga, Y. Matsushita, Y. Ueda, and T. Niina, in *Amorphous and Crystalline Silicon Carbide and Related Materials II*, M. M. Rahman, C. Y.-W. Yang, and G. L. Harris, Eds., Vol. 43 (Springer-Verlag, Berlin, 1989).
9. G. K. Reeves, Solid State Electronics **21**, 801 (1978).

10. E. N. Mokhov, Y. A. Vodakov, G. A. Lomakina, Soviet Physics - Solid State **11**(2), 415 (1969).
11. C. van Opdorp, Solid State Electronics **14**, 613 (1971).
12. E. Mokhov, Y. A. Vodakov, G. A. Lomakina, V. G. Oding, G. F. Kholuyanov, and V. V. Semenov, Soviet Physics - Semiconductors **6**(3), 414 (1972).

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